

April 30, 2004



To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/785,522 02/24/04 |

Yue-Der Chih

AN ARRAY STRUCTURE OF TWO-TRANSISTOR CELLS WITH MERGED FLOATING GATES FOR BYTE ERASE AND RE-WRITE IF DISTURBED ALGORITHM

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

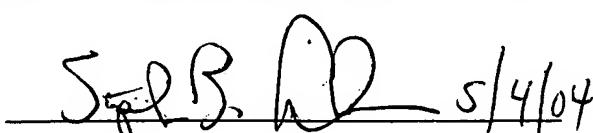
The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 5/4/04

U.S. Patent 6,376,876 to Shin et al., "NAND-Type Flash Memory Devices and Methods of Fabricating the Same," discusses a NAND type flash memory array that uses a low resistance common source line with low aspect ratio bit line contact holes.

U.S. Patent 6,400,603 to Blyth et al., "Electronically-Eraseable Programmable Read-Only Memory Having Reduced-Page-Size Program and Erase," discusses a flash EEPROM array directed to the reduced size of blocks or pages that are to be erased in a write or an erase operation.

U.S. Patent 6,128,220 to Banyai et al., "Apparatus for Enabling EEPROM Functionality Using a Flash Memory Device," discusses a flash memory device that provides a byte-alterable nonvolatile memory.

U.S. Patent 6,121,087 to Mann et al., "Integrated Circuit Device with Embedded Flash Memory and Method for Manufacturing Same," discloses an integrated circuit device with an embedded EEPROM memory.

U.S. Patent 6,088,269 to Lambertson, "Compact Page-Erasable EEPROM Non-Volatile Memory," discloses a compact page erasable EEPROM without the use of the control gate to improve electron tunneling efficiency during programming.

U.S. Patent 5,812,452 to Hoang, "Electrically Byte-Selectable and Byte-Alterable Memory Arrays," discloses a byte selectable and byte alterable memory array.

U.S. Patent 5,544,103 to Lambertson, "Compact Page-Erasable EEPROM Non-Volatile Memory," discloses a compact, electrically erasable and programmable nonvolatile memory device which has unique programming and erasing techniques in which the control gate is eliminated as a means for improving electron tunneling efficiency.

U.S. Patent 5,033,023 to Hsia et al., "High Density EEPROM Cell and Process for Making the Cell," discusses an EEPROM directed to a byte erase operation.

Sincerely,


Stephen B. Ackerman,
Reg. No. 37761

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION.

MAY 06 20

(Using approval shoulds if necessary)

Doctor Number (Optional)

TSMC-02-115/320

1916 COAST SURVEY

10/785,522

Appleton

"Yue-Der Chih"

Flying Dutch

02/24/04

Grow At Home

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U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER DOCUMENTS (including Author, Title, Date, Portion or Pages, Etc.)

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DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.